In-plane Thermoelectric Properties of Si/Ge Superlattice

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Abstract

In this paper we report experimental investigation of the in-plane thermoelectric properties of Si/Ge superlattices grown on silicon-on-insulator wafers. A two-wire 3 ω method was employed to measure the in-plane thermal conductivity of the superlattice sample investigated. The in-plane Seebeck coefficient and electrical conductivity of the same sample are also measured. Experimental data are compared with the results of theoretical models of carrier transport based on carrier pocket engineering and partial diffuse phonon interface scattering.

1. Introduction

The thermoelectric properties of low-dimensional structures, particularly superlattices, have received much attention in recent years [1]. Theoretical investigation has demonstrated that the optimum ZT value in low-dimensional system will be enhanced due to the density of states change [2]. The figure-of merit-enhancement has been proved experimentally on PbTe/Pb_{1-x}Eu_xTe multiple quantum well system [3,4]. Recent theoretical studies considering multivalley degenerate and lattice strain bandgap regulation, called the carrier pocket engineering, give another direction to optimize the thermoelectric properties [5,6]. A series of Si/Ge superlattice samples has been designed and fabricated based on this concept and corresponding experimental investigation has been carried to testify it [6]. Besides the electronic contribution to the

ZT enhancement, the lattice thermal conductivity can be greatly reduced in the low-dimensional systems. This also plays an important role in enhancing the figure of merit [7]. From the experimental point of view, the anisotropy in transport properties requires characterization of thermoelectric properties at certain direction. However, due to the difficulties associated with thin film property characterization, it is difficult to have both electrical and thermal properties measured in one direction. In this paper, we will report our investigation of thermoelectric properties of Si/Ge superlattice in the direction parallel to the film plane, i.e., the in-plane direction. The in-plane thermal conductivity of the superlattice is measured by a 2-wire 3 ω technique and the in-plane Seebeck coefficient and electrical conductivity are measured with conventional temperature gradient and four-point-probe method. The ZT values in the temperature range from about 100K to 300K are then calculated from the measured data. The results are compared with the theoretical model applying the carrier pocket engineering concept.

2. Sample Description

To investigate the carrier pocket engineering in optimizing thermoelectric performance, a series of symmetrically strained Si(20Å)/Ge(20Å) superlattice samples with different doping and periods (up to 100) have been grown and measured electrically at in-plane direction [6] and thermally at cross-plane direction [8] before. In this paper, we measured a sample that belongs to the same

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series but has more periods. The sample, labeled JL215, was grown by solid source molecular-beam-epitaxy (MBE), on a (100) oriented silicon-on-insulator (SOI) substrate. To obtain symmetrically strained Si/Ge superlattice, a SiGe alloy buffer layer was grown first to accommodate the lattice mismatch between Si and Ge. The buffer contains a 500 Å Si layer, followed by a 1 μm continuously graded Si_{1-x}Ge_x alloy layer with x increasing from 0 to 0.5 and a 0.3 μm Si_{0.5}Ge_{0.5} alloy layer. The superlattice part contains a 300-period Si(20Å)/Ge(20Å) layer. The total thickness of superlattice layer is thus 1.2 μm. The superlattice layer was homogeneously doped with Sb to about 1×10¹⁹ cm⁻³. To facilitate the measurement, a sample that has only the buffer part was grown and labeled as JL214. The buffer sample was used as a reference for subtraction purpose, as described in the following section.

3. Experimental Procedure

3.1 Thermal conductivity

A 2-wire 3ω method was used to measure the anisotropic thermal conductivity of the superlattice sample. The 3ω technique has been widely used in measuring thermal conductivity of bulk substrate or thin film at cross-plane direction [10]. Based on the same principle, the 2-wire differential 3ω technique was developed for measuring anisotropic thermal conductivity of thin film [9]. More information on this method can be found in Ref. 9. Here we briefly describe the principle of the measurement method. To determine the anisotropic thermal conductivity of the thin film, we use two heater-temperature sensors with different wire width to sense the temperature response of the sample. Based on the 2-dimensional heat conduction model, the in-plane and cross-plane thermal conductivities can be determined from the temperature rise signal from the two wires. To obtain the thermal conductivity of the Si/Ge superlattice, the measurement was conducted on 3 samples, JL215, JL214 and a piece of SOI wafer. The buffer JL214 and SOI sample are used as references. On all three samples, a 100nm-thick PECVD SiN_x layer was deposited to provide electrical insulation for the measurement. For each sample, two 3ω heater-sensor wires, with widths 2 μm and 30 μm respectively, were patterned and deposited by e-beam evaporation and lift-off process. The measurements were conducted inside a vacuum cryostat that operated from 80K to 300K. The AC temperature signal at modulated frequency from 700 to 3000Hz are collected and recorded. Data reduction is carried out with a fitting program, which is developed based the on two-dimensional heat conduction model. The in-plane and cross-plane thermal conductivities of the superlattice layer are determined through such data reduction.

3.2 Seebeck coefficient and electrical conductivity

Fig. 1 shows the sample configuration for experimental measurement of Seebeck coefficient S and electrical

conductivity σ . The sample to be measured is cut into 5mm×25mm rectangular shape. On the surface of the sample, there are two current input bars near the two ends of the sample. The distance between the two bars is about

Figure 1. Schematic picture of Seebeck coefficient and electrical conductivity measurement setup

20mm. In between the two bars, two thermocouples separated 10-12mm apart are attached to sample. Each thermocouple is 5mm away from the current input bar at the same side. At the bottom of the sample, a heater is attached at one side. The Seebeck coefficient is measured by the well-established temperature gradient method. The heater is used to create in-plane temperature gradient between the two points and the two thermocouples are used to measure both the temperature and Seebeck voltage. The Seebeck coefficient is obtained from the slope of temperature gradient-Seebeck voltage curve. The electrical conductivity is measured from the I-V measurements. A small DC current is input from the current bars to flow uniformly across the sample, and the voltage between the middle two points are taken from copper wires of the two thermocouple. To realize ohmic contacts, electrically contacting area such as the current bars and sensing points were patterned with e-beam deposited Sb/In and annealed at 300°C for 1 minute. The current input wires and thermocouples are attached to the sample using Indium. The whole setup was also put into vacuum cryostat that operates from 80K to 300K. After measuring both samples JL215 and JL214, a subtraction process is required to obtain the S and σ of the superlattice layer. Based on the sample structure, simple parallel resistance and source models are used in subtraction to eliminate the buffer effect for the superlattice properties.

$$\sigma_{SL} = \frac{\sigma_{JL215} D_{JL215} - \sigma_{JL214} D_{JL214}}{D_{JL215} - D_{JL214}}$$

$$S_{SL} = \frac{S_{JL215} \sigma_{JL215} D_{JL215} - S_{JL214} \sigma_{JL214} D_{JL214}}{\sigma_{JL215} D_{JL215} - \sigma_{JL214} D_{JL214}}$$

where S_{JL215} , σ_{JL215} are Seebeck coefficient and electrical conductivity measured from sample JL215, S_{JL214} , σ_{JL214} are those measured from sample JL214, and D_{JL215} and D_{JL214} are the total thickness of the two samples respectively.

4. Results and analysis

The in-plane and cross-plane thermal conductivities of the superlattice layer are plotted in Fig.2. The experimental data are compared with theoretical modeling results. The

Figure 2. Cross-plane and in-plane thermal conductivities of Si/Ge superlattice measured by 2-wire 3ω method and results of theoretical modeling considering partial diffuse interface scattering

Figure 3. Seebeck coefficient of the superlattice, before and after buffer effect subtraction. Inset is the Seebeck coefficient variation with carrier concentration, experimental and theoretical data. [Ref. 6]

theoretical model, developed by Chen [7,11], is the solution of phonon Boltzmann transport equation that considers partial diffuse scattering at interface by applying a specularity parameter “p”. The parameter “p” varies from 0 to 1, corresponding to the interface scattering variation from totally diffuse to totally specular. In the cross-plane direction, the model fits the experimental data quite well with specularity parameter p about 0.6. In the in-plane direction, the model can capture the trend and fit most data with specularity parameter p between 0.5 and 0.6. This indicates that the partial diffuse interface scattering is the major mechanism to cause thermal conductivity reduction of the superlattice structure. Detailed analysis and comparison with effective bulk thermal conductivity based on Fourier law presented elsewhere [12]. The analysis shows that the cross-plane thermal conductivity can be reduced by two orders of magnitude and the in-plane

Figure 4. Electrical conductivity of the superlattice, before and after buffer effect subtraction

Figure 5. In-plane ZT and power factor of the Si/Ge superlattice

thermal conductivity can be reduced to that of alloy with equivalent composition. The Seebeck coefficient (absolute value) and electrical conductivity of the superlattice are shown in Fig.3 and Fig. 4 respectively. The inset in Fig. 3 shows the measured room temperature Seebeck coefficients varies with carrier concentration and the theoretical modeling of Koga et al. [6]. The theoretical model considers the quantum confinement effects in different carrier pockets and includes the strain effect on the band-edge alignment. The constant relaxation time approximation (CRTA) is used, together with the introduction of an extrinsic scattering term τ_{ext} to fit the experimental data. We didn't measure the carrier concentration of JL215. Based on the doping concentration and previous measurements, we assume it to be around $1.5 \times 10^{19} \text{ cm}^{-3}$. By using this value, the Seebeck coefficient obtained from JL215 can be fitted using the model. Fig. 5 shows the in-plane ZT and the power factor $S^2\sigma$ in the

temperature range from about 100K to 300K. At room temperature, the ZT value measured is 0.047, which is about 4 times higher than the optimum value of bulk Si [2]. The power factor at room temperature is about $10 \mu\text{W}/\text{cmK}^2$, which also close to the value reported by Koga et al. [6]. According to Ref. 6, the power factor at room temperature without extrinsic scattering is about $35 \mu\text{W}/\text{cmK}^2$. The extrinsic scattering, possibly from interface roughness, need to be investigated further in future efforts to optimize the thermoelectric performance of superlattice structures.

Conclusion

We measured the in-plane thermal conductivity, Seebeck coefficient and electrical conductivity of a Si/Ge superlattice sample. The thermal conductivity is greatly reduced in both in-plane and cross-plane direction and can be fitted well with theoretical modeling considering partial diffuse interface scattering. The Seebeck coefficient and power factor data are in reasonable agreement with the carrier pocket engineering model. The in-plane ZT values from 100K to 300K are calculated based on measured thermoelectric properties. The ZT value obtained is about 4 times higher than the optimum ZT value of bulk Si. More efforts are required to investigate the extrinsic scattering in order to further optimize the thermoelectric performance.

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