Computer Simulation of Charging and Erasing Transients of a Ge/Si Hetero-nanocrystal-based Flash Memory

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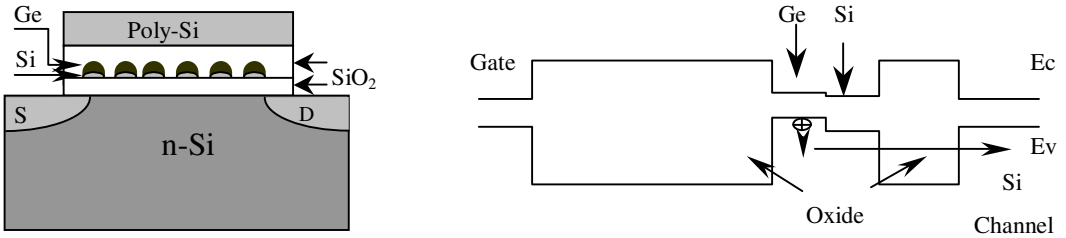
ABSTRACT

The transient process of the programming and erasing is very important for a nanocrystal-floating-gate flash memory. In this work, a computer simulation was carried out to investigate the charging, retention and erasing processes of our proposed Ge/Si hetero-nanocrystal floating gate flash memory. The transient gate current, the transient drain current and the average charge in one dot were simulated respectively. Evident hysteresis features can be observed in the transient processes in a voltage-sweeping measurement mode. While measuring the transient process in a constant voltage mode, the time decay of transient current and charge are weakened if Ge is used on the Si dot, indicating a longer retention time for Ge/Si-floating-gate flash memory.

INTRODUCTION

As the discrete storage nodes to replace conventional continuous metal or poly-Si floating gate in a metal-oxide-semiconductor-field-effect-transistor (MOSFET), Si nanocrystals offer the advantages of smaller device size, faster programming and lower voltage [1-5], which enables Si nanocrystal floating gate flash memory a promising candidate to continue the scaling of FLASH devices. In such a Si nanocrystal-based memory device, since the tunneling oxide is very thin, the simultaneous realization of a long retention time as well as a high programming/erasing speed is important. The quantum confinement effect raises the energy levels of the Si nanocrystal and degrades the retention. A trap-enhanced retention model has been proposed by Shi *et al* [3], [4] and She *et al* [6] to explain the long retention. However, the trap-enhanced storage is sensitive to the operation temperature [3], [4] and the trap level [6] which are difficult to control in fabrication leading to inconsistency in device performance, especially for the device containing only several or even one nanocrystal storage node. Recently, Ge/Si hetero-nanocrystals was proposed to replace Si nanocrystals as the floating gate [7] for a p-channel memory. The device structure and the band structure are shown in Fig. 1. It is developed in this work to include both



(a) (b)

Figure 1. (a) The schematic diagram of the p-channel Memory device using Ge/Si as floating gates. (b) The energy band structure of the memory.

electron and hole charging/discharging transient processes. The basic idea there was to use the quantum well formed by the control oxide/Ge/Si to confine a hole in the Ge dot. Since Ev of Ge is lower than that of the Si dot, the hole has to penetrate two barriers during the tunneling-back process to the substrate, i.e., the Ge/Si band offset and the Si/SiO_2 band offset. Therefore, the escaping probability can be tremendously depressed by the additional Ge dot as quantum well. Moreover the erasing and writing speed will not be influenced by the presence of the Ge dot on top of the Si dot since the barrier only results from the oxide barrier.

A Ge/Si hetero-nanoscrystal memory responds in a different way compared to a Si nanocrystal memory if Coulomb blockade effect is considered and hence it is necessary to compare the dynamic charging/discharging behavior of a Ge/Si heter-nanocrystal memory with a Si nanocrystal memory. Additionally, the understanding of the transient process is also important for a Si nanocrystal memory, for which the corresponding theoretical investigation is still lacking although there have been many experimental observations, such as the transient processes reported for the source-to-drain current [8], charge density [9], or capacitance [10]. However, the most often assumed trend of transient processes in these literatures is an exponetial growth or exponential decay law. This is questionable since the Coulomb blockade effect results from the charge in the nanocrystal will also contribute to the discharging. The motivation of this work is to reveal the time-dependent processes of a Ge/Si hetero-nanocrystal memory, including the kinetics of the gate leakage current in retention, the programming/erasing current, the source-drain current and the threshold voltage shift. The influence of the gate voltage, the tunneling oxide thickness and the dot size are investigated as well. The comparison between a Ge/Si and a Si nanocrystal memory is also made.

THEORY AND MODEL

All of the time-related transient processes in this work are based on this simple equation:

$$Q(t+\Delta t) = Q(t) \pm I_t \times \Delta t \tag{1}$$

where Q, t, Δt and I_t are the charge in the nanocrystal, the time, the time step and the transient tunneling current, respectively. During each step, the electrical potential and tunneling probability [11] are derived by solving Poisson equation numerically with the presence of the charge in the nanocrystal.

The tunneling current density for erasing and programming is [12]:

$$J = q\int_{E_{shift}\le E} T(E) f(E) \rho(E) F(E) dE \tag{2}$$

where $f(E)$ is the impact frequency, $\rho(E)$ the 2-dimensional (2-D) density of states, $F(E)$ the Fermi-Dirac distribution function and $T(E)$ the tunneling probability, respectively. E_{shift} is the Si valence (for writing process) or conduction band (for erasing process) shift due to the quantum confinement effect from the small size of the nanocrsytal.

The retention time (τ) is derived from the following expression:

$$\tau = \frac{1}{\sum_{i=n}^{\infty} \exp\left(\frac{-(E_i - E_1)}{k_B T}\right) f(E_i) T(E_i)} \tag{3}$$

where E_i, E_1, K_B are the i-th excited state and ground state (for holes) in the hetero-nanocrystal and Boltzmann's constant, respectively. 'n' is the quantum number from which the wave function of the hole spreads over both Ge and Si regions of the hetero-nanocrystal. The eigen-energy levels and corresponding wave functions are calculated using an improved shooting method [13] with the effective mass approximation. For all the calculations, the control oxide is fixed as 5 nm so that the tunneling through control oxide can be disregarded.

Based on a linear model using a small drain-to-source voltage, the transient source-to-drain current (I_{DS}) is calculated as a function of time. In our simulations, both the length and width of the channel are assumed to be 1 μm, the mobility μ_{Surf} is taken as 400 $cm^2/V \cdot s$ and V_{DS} is 0.01 V.

RESULTS AND DISCUSSION

The writing transient process is shown in Fig. 2 (a) for the charge written (Q_{Dot}) in one storage node. The tunneling oxide thickness (T_{ox}) is 2.0 nm. The thicknesses of the Ge dot and the Si dot are 5 nm and 3 nm, respectively. Note the writing saturation in Fig. 2 due to the Coulomb repulsion from the charged dot that raises its potential energy and repels the subsequent hole. It is seen that for a small V_g after a rapid growth at the very beginning, Q_{Dot} tends to be a constant that depends on V_g with a positive correlation. This V_g dependent Q_{Dot} then results in a V_g dependent threshold voltage shift (ΔV_{th}), as shown in Fig. 2 (b) where ΔV_{th} is plotted as a function of writing V_g. It indicates that ΔV_{th} grows with writing V_g, from ΔV_{th} = 0.6 V at V_g = -2.0 V to ΔV_{th} = 0.9 V at V_g = -5 V. However, it is observed that ΔV_{th} approaches to a constant when $|V_g| > 4$ V. This is owed to the self-limited writing at the lower gate voltage. Due to the small nanocrystal size, the charge density inside the dot can be as high as ~ 10^{19} cm^{-3}, which not only raises the potential of the nanocrystal significantly but also screens the electrical field from the control gate. Therefore, the potential drop across the tunneling oxide is remarkably reduced, leading to the fact that the charging process slows down considerably. However, the charge-induced potential cannot balance the potential from the control gate when the gate bias is high enough, i.e., -4 V in our case. Note that the charge not only increases the electrostatic potential of the quantum dot, but also raises the energy level for the second hole to occupy. Therefore, ΔV_{th} is saturated before the gate voltage becomes high enough to inject the second hole.

ΔV_{th} for a Ge/Si hetero-nanocrystal memory depends not only on V_g and the dot density, but also on the Ge/Si dot size. For a fixed the control oxide thickness (5 nm in our cases), larger Ge dot will introduce larger ΔV_{th}, which in consequence depresses the writing process more remarkably than smaller Ge dots. The transient writing current and I_{DS} at –6 V is shown in Fig. 3 (a) and (b) for Ge dot size of 3, 4 and 6 nm. The thickness of the tunneling oxide and the Si dot are 2 nm and 3 nm, respectively. Essentially, there are two factors determining I_{DS} in charging process, namely, the initial writing current and the Coulomb blockade effect. At t = 0, the two curves (for Ge=3 nm and 6 nm) have almost the same I_{DS}. However as time increases, a larger Ge dot leads to a greater I_{DS}, indicating that a larger Ge dot more significantly depresses the writing current during programming. Nevertheless, as shown in Fig. 3 (a), a larger Ge dot leads to a lower writing speed. Therefore, less charge is written to a larger nanocrystal than that of a smaller nanocrystal after the same writing time. In other words, it is more difficult to program a memory with larger Ge dots, as also shown in Fig. 3 (c), where the charge written to a dot is plotted against the charge time. Note that as shown in the inset of Fig. 3 (b), the time dependent I_{DS} does not follow an exponential decay law as has been assumed for a defect-free memory [8].

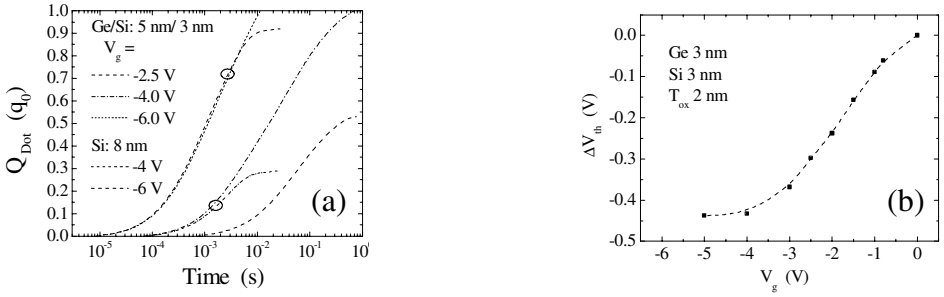


Figure 2. Writing process with the gate voltages ranging from –2 V to –7 V. (a) the charge written to a dot as a function of bias stress time and (b) the saturated threshold voltage shift as a function of the writing voltage.

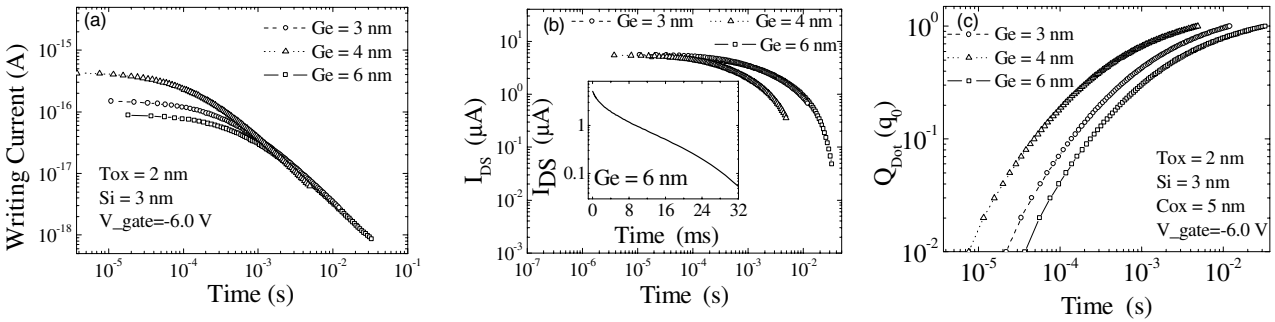


Figure 3. Role of Ge dot sizes in data writing at –6 V: (a) the writing transient current, (b) the source-to-drain currents and (c) the charge written to a dot. The inset in (b) indicates a non-exponential decay feature for the source-to-drain current. The tunneling oxide is fixed at 2 nm. q_0 in Fig. 3 (c) is the elemental charge.

The erasing transient characteristics are shown in Fig. 4 (a) for the current and (b) for the charge remaining in the nanocrystal Q_{Dot} with V_g ranging from 4 V to 7 V. The thicknesses of the Ge dot, the Si dot and the tunneling oxide are 5 nm, 3nm and 2 nm, respectively. The erasing current for V_g = 7 V is 30 times greater than that for V_g = 4 V at the very beginning of erasure. Nevertheless, the difference soon diminishes. For charge remaining in the dot, one finds that after some time lapse, the differences between different curves approaches to constants. The time to erase a hole is around 2×10^{-7} s for V_g = 7 V. There is not erasure saturation observed. Similar to writing process, the erasure process also does not obey exponential law, as shown in the inset in Fig. 4 (a).

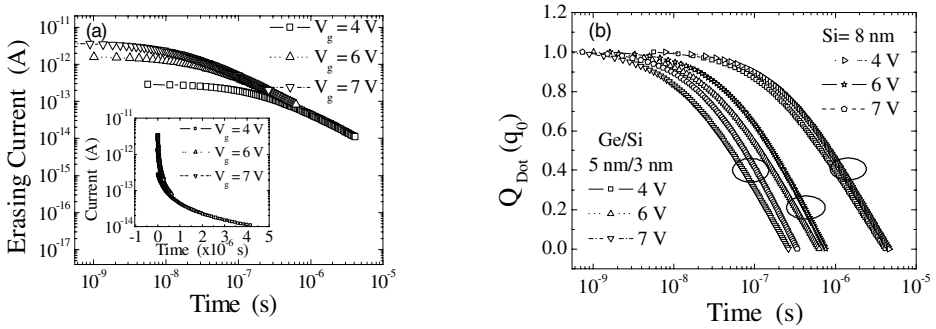


Figure 4. Erasure transients: (a) the erasing current and (b) the charge remaining in a dot. The inset in (a) indicates a non-exponential decay feature for the erasing current.

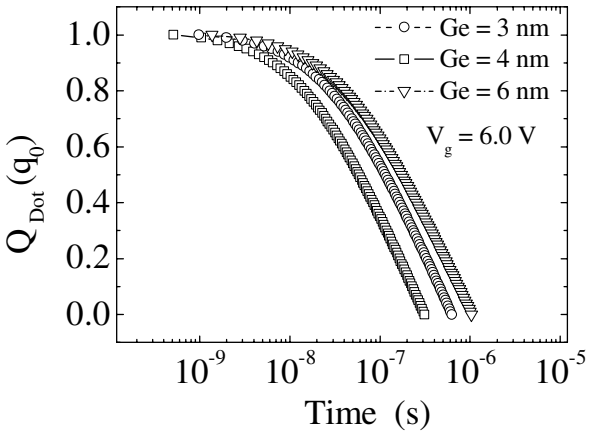


Figure 5. The charge remaining in the nanocrystal as a function of erasing time for different Ge dot sizes.

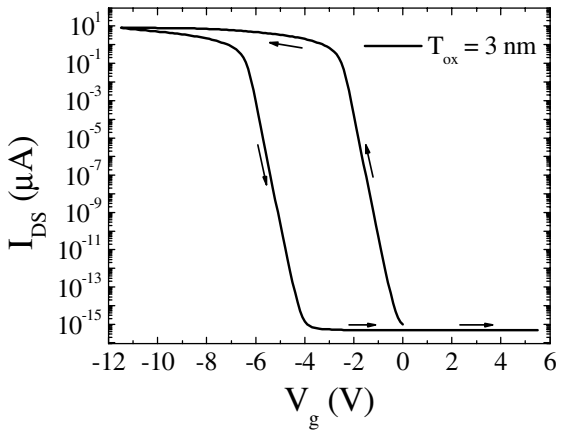
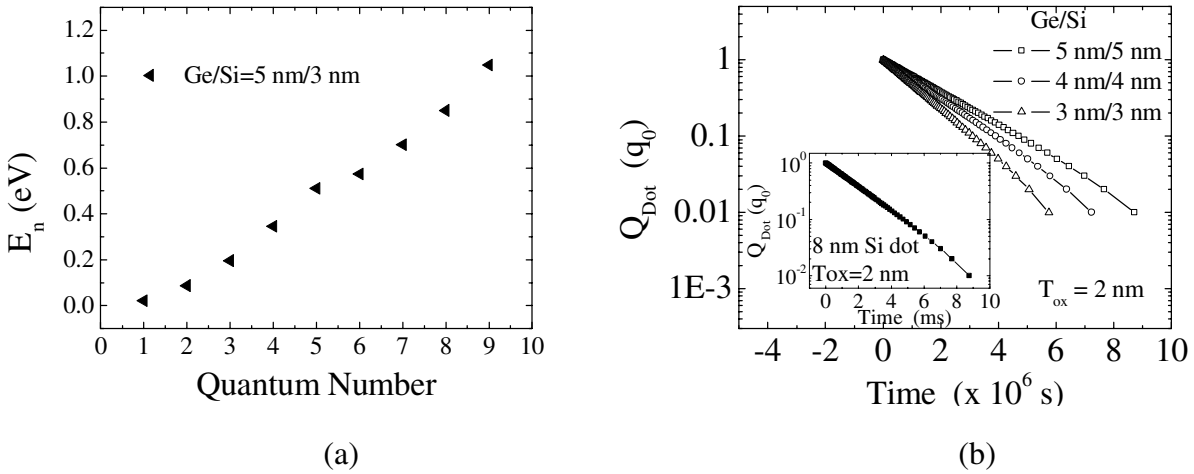


Figure 6. Hysterisis loop of I_{DS} in a voltage sweep mode. The tunneling oxide is 3 nm.



(a) (b)

Figure 7. (a) The eigenenergy levels for a Ge/Si hetero-dot. (b) Retention characteristics of the hetero-nanocrystal memory and the Si nanocrystal memory.

The effect of Ge dot size on the erasing process is investigated in Fig. 5 for the charge remaining in the nanocrystal with the Ge dot sizes are 3, 4 and 6 nm, respectively. The Si dot size is 3 nm and the tunneling oxide thickness is 2 nm. Very similar to the role of Ge dot size in the writing process, a larger Ge dot introduces a smaller erasing current and the difference is diminished as time progresses. The time for erasing one hole with Ge = 3 nm is almost 3 times faster than that with Ge = 6 nm.

A simulated voltage sweeping (2.0 V/s) measurement is plotted in Fig. 6, where the thickness of the Ge dot and the Si dot are 3 nm each with T_{ox} fixed at 3 nm. The sweeping continues forward until I_{DS} reaches a saturation value. Then the voltage sweeps back. A hysterisis feature can be seen, indicating the charging of electrons and holes from the substrate to the quantum dot.

The energy levels of the Ge/Si dot and the retention transient are presented in Fig. 7. The retention characteristic of a Si nanocrystal memory is shown as well. The energy levels as a function of the quantum number clearly exhibits a two-region quantum well formed by the Ge/Si

hetero-nanocrystal. It is observed that the retention time of a Si nanocrystal memory is only ~ 1 ms while it is almost 10^9 times longer if a 5 nm Ge is added onto the top of Si dot.

CONCLUSION

The roles of the Ge/Si dot size and the gate voltage on the programming/erasing and retention transient characteristics are investigated. Compared with a Si nanocrystal memory, a Ge/Si hetero-nanocrystal improves the retention characteristics dramatically without significantly influencing the programming/erasing speed. Larger nanocrystals result in lower writing and erasing speeds and a slower charge loss speed. The ultimate charge in one nanocrystal that can be written at a fixed gate voltage is a function of the gate voltage and a larger threshold voltage shift can be achieved with a higher writing voltage. Both the transient writing current and the source-to-drain current do not exhibit exponential dependence on bias stress time.

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