Threshold Voltage Shift in Hetero-nanocystal Floating Gate Flash Memory

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ABSTRACT

The threshold voltage shift of a p-channel Ge/Si hetero-nanocrystal floating gate memory device was investigated both numerically and phenomenologically. The numerical investigations, by solving 2-D Poisson-Boltzmann equation, show that the presence of the Ge on Si dot tremendously prolongs the retention time, reflected by the time decay behavior of the threshold voltage shift. The increase of the thickness of either Si or Ge dot will reduce the threshold voltage shift. The shift strongly depends on the dot density. Nevertheless, only a weak relation between the threshold voltage shift and the tunneling oxide thickness was found. A circuit model was then introduced to interpret the behavior of threshold voltage shift, which agrees well with the results of the numerical method.

INTRODUCTION

Si nanocrystal floating gate memory has been a promising candidate to replace the current FLASH memories for its faster speed, lower power consumption and compatibility to traditional complementary metal-oxide-semiconductor processing [1-4]. Due to the ultra thin tunneling oxide in this memory, the trade-off between a high programming speed and a long retention time is now challenging. To solve this issue, Ge/Si hetero-nanocrystals has been proposed to replace the Si nanocrystals [5]. Owing to the band offset of Ge/Si, a flash memory using hetero-nanocrystals as floating gate exhibits a much longer retention time while keeping almost the same programming speed [6]. The threshold voltage shift ΔV_{th}, as an index of memory window, is one of the most important parameters for the flash memory [7]. In this work, the dependences of ΔV_{th} on nanocrystal size, density and tunneling oxide thickness are studied for a p-channel Ge/Si hetero-nanocrystal memory, with both a numerical method and an equivalent circuit method. Good consistencies were found between these two methods.

DEVICE STRUCTURE AND MODEL

Ge/Si hetero-nanocrystals are embedded in the oxide layer between the control gate and the n-type Si substrate, forming a p-channel Ge/Si hetero-nanocrystal memory device. Fig.1 is the simulation cell used in the numerical investigation, which is a symmetric sub-cell of an actual memory device.

The electrical potential ϕ satisfies the Poisson-Boltzmann's equation:

$$\nabla \bullet (\varepsilon \nabla \phi) = -q(p - n + D) \qquad (1)$$

where q, ε, n and p are the elementary electron charge, the material permittivity, the mobile electron and hole densities, respectively, and D is the concentration of ionized impurities (n-type

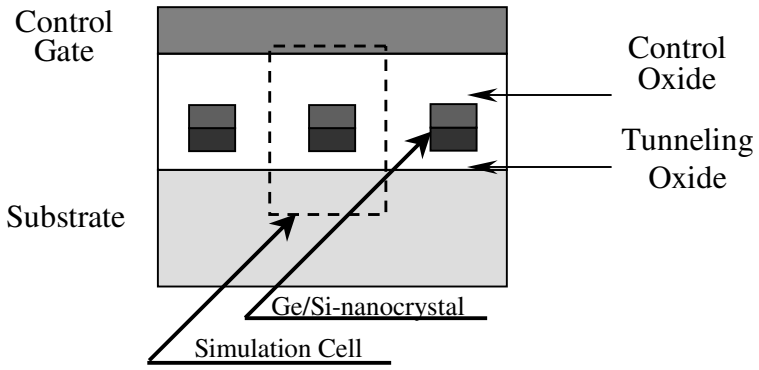

Figure 1. Simulation cell with a periodic boundary condition in lateral direction

doping). The potential and charge density was calculated with the 2-dimensional finite difference iterative method. The thickness sum of the Si dot, Ge dot and the control oxide is kept a constant at 10 nm in all simulations. The threshold voltage is defined as the gate voltage when the minimum hole density (along the channel direction) at the Si/SiO_2 interface reaches the electron density (doping concentration) in the n-type substrate. For simplicity, the control gate contact and substrate contact were treated as ideal ohmic contacts.

In the device model, the simulation cell was regarded as the combination of several parallel plate capacitors, as shown in Fig.2. ΔV_{th} can be then evaluated as:

$$\Delta V_{th} = \frac{\Delta Q_{eff}}{C_{total}} \tag{2}$$

where C_{total} and Q_{eff} are defined in equations (3) and (4) [8], respectively:

$$\frac{1}{C_{total}} = \frac{1}{C_{21}} + \frac{1}{C_{22}} + \frac{1}{C_{23}} + \frac{1}{C_{24}} \tag{3}$$

$$Q_{eff} = \frac{\varepsilon_{ox}}{d}\int_0^d \frac{x\rho(x)}{\varepsilon(x)}dx \tag{4}$$

Here, C_1 is the mutual capacitance between the control gate and the channel area that is not covered by the nanocrystals. C_{21}, C_{22}, C_{23} and C_{24} are the mutual capacitances between the control gate and the Ge dot, the self-capacitances of the Ge dot and Si dot, and the mutual capacitance between the Si dot and the channel, respectively. Q_{eff} stands for the effective charge at the Si/SiO_2 interface induced by the charge in the nanocrystal. This concept of effective charge is very similar to the case of a MOSFET with fixed charge in the oxide insulator [8] where the location of the fixed charge in the oxide contributes to the threshold voltage.

RESULTS AND DISCUSSION

The retention time sensitively depends on the tunneling oxide thickness and the presence of the Ge dot on top of the Si dot [6]. In our calculation, in order to achieve a 10-year retention, a 2.07-nm-thick tunneling oxide is needed for Si (2 nm) nanocrystal memory, while for the Ge/Si (3nm/2nm) hetero-nanocrystal memory the tunneling oxide can be as thin as 1.36 nm. In Fig. 3,

ΔV_{th} is shown at different tunneling oxide is needed for Si (2 nm) nanocrystal memory, while for the

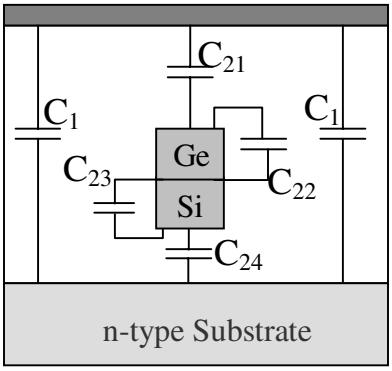

Figure 2. The diagram of the equivalent circuit model for the flash memory, with several parallel plat capacitors representing the memory cell.

Ge/Si (3nm/2nm) hetero-nanocrystal memory the tunneling oxide can be as thin as 1.36 nm. In Fig. 3, ΔV_{th} is shown at different time of charge storage for the cases with and without the Ge dot on top of the Si nanocrystal, respectively. It is found that if only Si nanocrystals are present and the thickness of the tunneling oxide is 2.07 nm (curve 1), ΔV_{th} immediately after the charge injection can be as high as -1.8 V. However, ΔV_{th} declines more rapidly than the case where the tunneling oxides are 1.36 nm (curve 2) with Ge/Si hetero-nanocrystals.

The ideal parallel plate capacitor model is used for all the capacitors in the equivalent circuit model. C_1 is not taken into account since the threshold voltage is decided by the part that is most difficult to be inverted. For both the Si and Ge nanocrystals, one can simply use the parallel plate capacitor model with the plate areas equal to the dot cross sections. However, the capacitor area for C_{24}, namely the area screened by the charge in the nanocrystal, is not straightforward although it has been discussed in Refs. 9 and 10, where the whole channel area is used as the screen area. However, it has been shown in our numerical calculation that this approximation using the whole channel area is only valid when the inter-dot distance is so small that the potential distribution over the whole channel is fairly uniform. Fig. 4 depicts the calculated surface potential along the channel (Source-Drain direction) for several inter-dot distances. The potential distribution is quite uneven with a larger dot-to-dot distances, thus the whole channel area cannot be accepted as the capacitor (C_{24}) area in our calculation when the equivalent charge

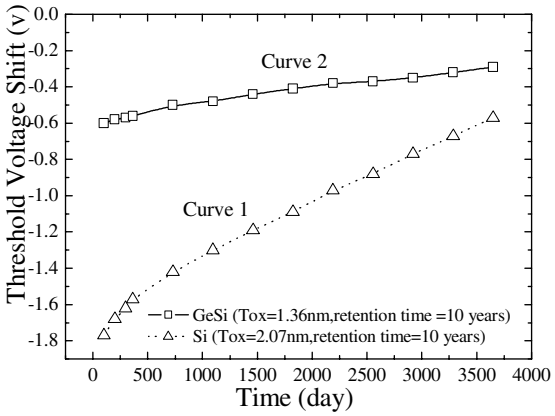

Figure 3. The threshold voltage shift as a function of storage time for two cases.

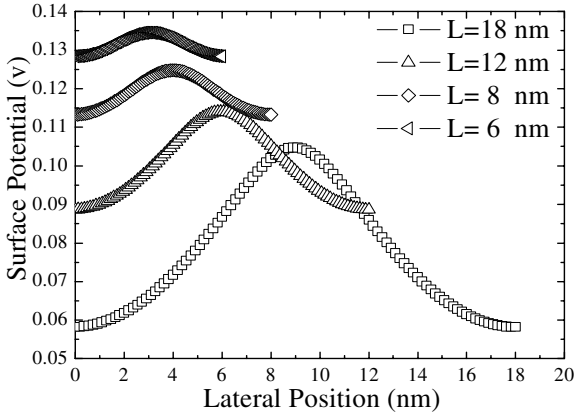

Figure 4. The potential distribution along the channel for different inter-dot distances (L) when the gate voltage is 0 V.

is used. Additionally, the potential not only distributes directly under the nanocrystal but also covers other parts of the channel. This fact indicates that the employment of only nanocrystal area is not suitable. Therefore, it is reasonable to use an effective area whose value falls between the areas of the whole device and nanocrystal. Since the derivation of an analytic value of the effective area is difficult, we have used numerical method for a phenomenological fitting here only.

In Fig. 5, ΔV_{th} is plotted as a function of dot density using the effective screening length of 0.3 times inter-dot distance, where the results with the whole device length and the nanocrystal size only are shown as well, all taking the data obtained from the numerical solution of Poisson's equation as the reference. $|\Delta V_{th}|$ increases from 0.38 V to 0.68 V as the dot density varies from 2.7×10^{11} cm^{-2} to 6×10^{11} cm^{-2}, corresponding to the dot-to-dot distance changing from 19 nm to 13 nm. It is evident now that the approximations using either the whole device area or using the nanocrystal size are not consistent with the data from Poisson's equation. Only the approximation using 0.3 times the inter-dot distance matches the data from the numerical calculations, particularly for the case of smaller dot densities.

The influence of the Ge dot size on ΔV_{th} is shown in Fig. 6 with the tunneling oxide 2.07 nm and lateral simulation cell size (L) 14 nm which corresponds to a dot density of 5×10^{11} cm^{-2}. Two Si dot (2 nm and 3 nm, respectively) sizes are investigated. One observes that ΔV_{th} decreases as either the Ge dot or Si dot thickness increases. The results from the equivalent circuit model with an effective screen length 0.3 L are also shown. They have an encouraging agreement.

The dependence of ΔV_{th} on the tunneling oxide thickness is presented in Fig.7 with the Si and Ge dots 2 nm and 3 nm, respectively. ΔV_{th} changes only about 0.05 V when the tunneling oxide thickness varies from 3 nm to 5 nm. Again the numerical method fits well the circuit model with an effective screen length 0.3 L.

The behavior of ΔV_{th} can be interpreted based on the circuit model. Since the charge is only in Ge dot, Eq. (4) can be simplified as:

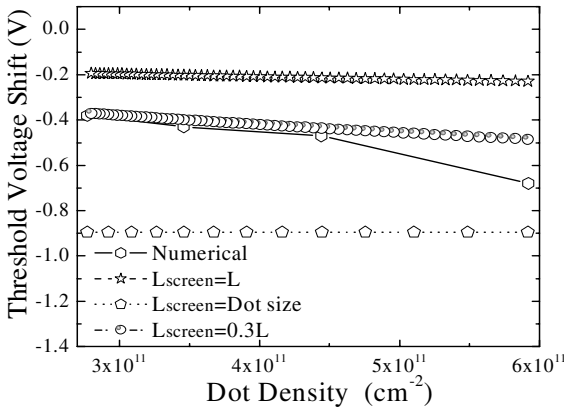

Figure 5. A comparison between the numerical method and the equivalent circuit model. The phenomenological effective screen lengths (L_{screen}) are chosen as L, 0.3 L and the Ge dot size in the equivalent circuit model, respectively. The result based on screen length of 0.3L matches the numerical data.

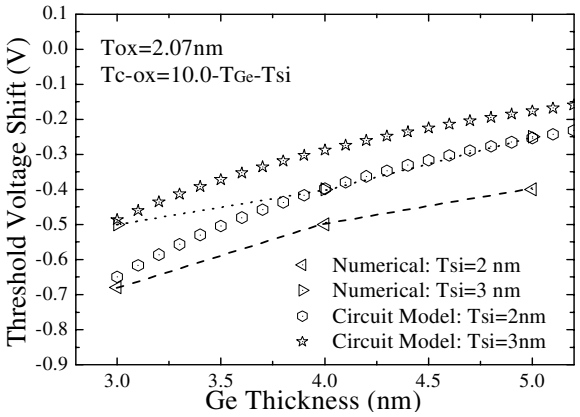

Figure 6. The threshold voltage shift as a function of the Ge dot thickness. Compared to the data from the equivalent circuit model with a phenomenological effective screen length 0.3 L.

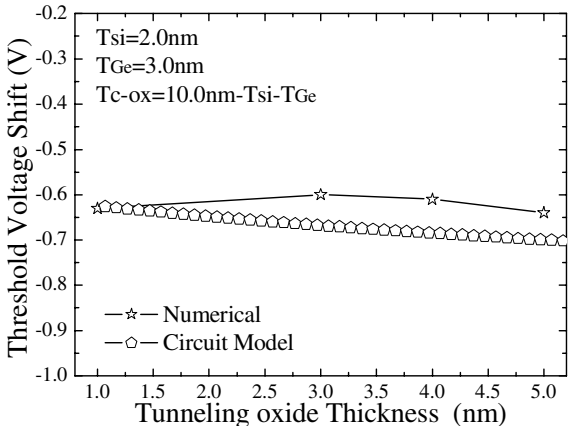

Figure 7. The threshold voltage shift as a function of the tunneling oxide thickness. Compared to the data from the equivalent circuit model with a phenomenological effective screen length 0.3 L.

$$Q_{eff} = \frac{\varepsilon_{ox} q}{\varepsilon_{Ge}} \times \frac{10\ nm - T_{Si} - 0.5T_{Ge}}{10\ nm + T_{ox}} \qquad (5)$$

where $T_{Si}+T_{Ge}+Tc\text{-}ox = 10$ nm is used with T_{Si}, T_{Ge}, Tc-ox the thickness of the Si dot, Ge dot and control oxide, respectively. It is evident that Q_{eff} decreases while C_{total} increases with an increase of either the Si dot or Ge dot thickness. The effect is then that greater Ge or Si nanocrystal thickness corresponds to a smaller ΔV_{th} since $\Delta V_{th} = \frac{\Delta Q_{eff}}{C_{total}}$. Since both C_{total} and Q_{eff} tend to get smaller as the tunneling oxide gets thicker, ΔV_{th} as their quotient exhibits a weaker dependence on the tunneling oxide thickness.

SUMMARY

The investigations of ΔV_{th} of a Ge/Si hetero-nanocrystal flash memory were carried out with both a numerical method and a simple circuit model. It was found that a larger shift could be achieved by decreasing the thickness of the Ge or Si nanocrystal. The shift increases with the dot density. However, the tunneling oxide thickness only slightly affects ΔV_{th}. Both the rigorous numerical method and the simple circuit model approximation of the threshold voltage shift exhibit a good consistence with each other.

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