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VSS-induced $NiSi_2$ Nanocrystal Memory

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ABSTRACT

$NiSi_2$ nanocrystals were synthesized and used as the floating gate for nonvolatile memory application. Vapor-solid-solid mechanism was employed to grow the $NiSi_2$ nanocrystals by introducing SiH_4 onto the Ni catalysts-covered SiO_2/Si substrate at 600˚C. The average size and density of the $NiSi_2$ nanocrystals are 7~10nm and 3×10^{11} cm^{-2}, respectively. Metal-oxide-semiconductor field-effect-transistor memory with $NiSi_2$ nanocrystals was fabricated and characterized. Programming/erasing, retention and endurance measurements were carried out and good performances were demonstrated.

INTRODUCTION

Silicide nanocrystals are believed as one of the promising candidates to replace traditional Si as the floating gates in nonvolatile memory. The time-voltage dilemma prevents conventional Si memory scale beyond 32nm technology node. Using silicide nanocrystals may extend this scale limit by enhancing the device retention without compromising the program efficiency. Because silicides are metallic materials, the strong coupling between the channel and floating gates helps improve the programming speed and deeper quantum well formed between the metals (those Fermi-levels within the energy band gap of Si), and Si substrate elongates the retention time. The storage capability can also be improved using silicide nanocrystals due to their high density of states. The large memory window makes it possible for the device to be used for multi-bit applications. Another advantage for silicide materials is their thermal stability. The current long retention reported in Si nanocrystal memory is mainly due to the charging on the defect levels within Si, which is not thermally robust.

Various silicide nanocrystals [1-5] have been reported showing good memory performance. The methods include ebeam evaporation, sputtering with post rapid thermal annealing (RTA). In this work, we use a novel method, i.e., Vapor-Solid-Solid (VSS), which is mainly used for nanowires growth [6-8], to synthesize silicide nanocrystals.

EXPERIMENT

A thin layer of metal Ni was deposited by ebeam evaporation on a 5nm thermally grown SiO_2 covered p-Si (100) substrate. In-situ annealing in N_2 at 900℃ for 30s was carried out to release the stress and densify the oxide film. The wafer was then transferred to a low vapor chemical vapor deposition (LPCVD) furnace for silicide synthesis. As the furnace temperature increases to the growth temperature, ~600℃, Ni nanocrystals were formed, then Si precursor (SiH_4) was introduced to diffuse into/react with Ni to form silicide. The growth time was calibrated and the SiH_4 gas was shut off at the time when no Si nanowires growth underneath the catalysts. Control oxide of 25nm was deposited on the nanocrystals followed by 350nm

polysilicon gate formation. Phosphorous was implanted to make heavily doped source/drain/gate regions. Aluminum was evaporated and patterned as the contacts to complete the fabrication. The device feature is 1μm.

RESULTS and DISCUSSION

Figure 1 shows the atomic force microscopy (AFM) image of $NiSi_2$ nanocrystals. The nanocrystal size is determined to be 7~10nm and the density is $3\times10^{11}cm^{-2}$. X-ray photoelectron spectroscopy (XPS) was used to ascertain the chemical composition of the nanocrystals to be $NiSi_2$ (Results are not shown here).

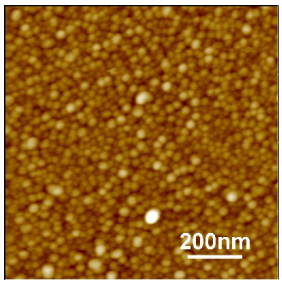

Figure 1 AFM image of $NiSi_2$ nanocrystals on SiO_2/Si substrate.

Figure 2 (a) shows the typical capacitance-voltage (C-V) sweep characteristics of $NiSi_2$ nanocrystals metal-oxide-semiconductor (MOS) memory. Nanocrystals are embedded between 5nm tunnel oxide and 25nm control oxide. The contact materials are aluminum. Three different scanning range, ± 5V, ± 8V, ± 10 V, have been applied to monitor the flat band voltage shifts as gate voltage sweeps. It is found that the memory window increases as scan voltage increases. With ± 5V scanning, memory window is 0.268V and with ± 10V scanning, memory window is 1.052V. Figure 2 (b) shows the sweep of a reference sample, where no nanocrystals are between control and tunnel oxide. Insignificant flat band voltage shift is observed, indicating the memory effect in $NiSi_2$ nanocrystal MOS memory is due to the electron charging in the nanocrystals, rather than interface/defect levels in the dielectric layers.

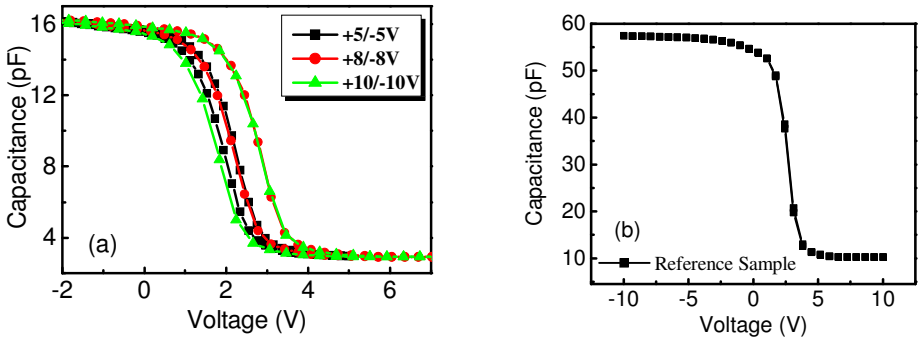

Figure 2 Capacitance-voltage (C-V) sweep of (a) MOS memory with $NiSi_2$ nanocrystals and (b) reference MOS device without any nanocrystals.

$NiSi_2$ nanocrystal metal-oxide-semiconductor field-effect-transistor (MOSFET) memory was fabricated using standard n-MOSFET process and the characterizations were carried out using Agilent 4155C semiconductor parameter analyzer to sense the threshold voltage and Agilent 81104A pulse/pattern generator to program/erase the memory. Figure 3 shows the charge retention performance of $NiSi_2$ nanocrystal memory after Fowler-Nordheim (FN) programming and erasing. The program and erase conditions are gate voltages of +20V and -20V, respectively, for 5 seconds. Retention performance at both programmed and erased states were recorded. After 10^5 seconds, the threshold voltage shifts change from 2.72V to 1.48V at programmed state and from -1.52V to -1.18V at the erased state, respectively. Ten-year retention is indicated in the figure to show that our device can survive ten years with memory window open. Figure 4 shows the endurance characteristics of the $NiSi_2$ nanocrystal memory. The device was charged and discharged by FN with V_G=18V/20ms and V_G=-18V/200ms, respectively. Up to 10^5 times of operation, the memory window shrinks from 1.749V to 1.351V, i.e. the charge loss after 10^5 time of programming/erasing is only ~23%.

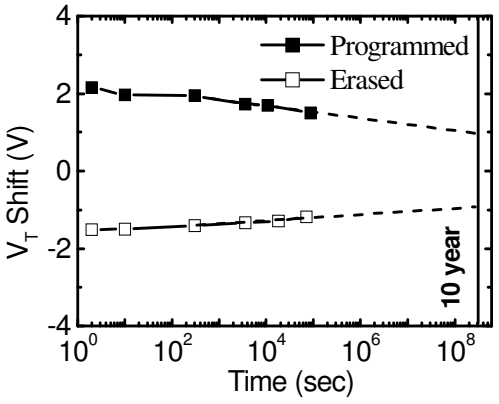

Figure 3 Retention characteristics of $NiSi_2$ NC memory at programmed and erased states

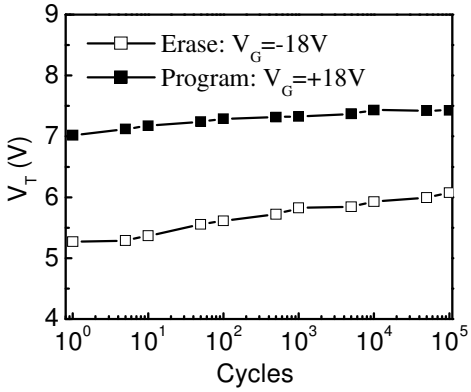

Figure 4 Endurance characteristics of $NiSi_2$ NC memory

In addition to FN, we also tried hot carrier injection to program the device, where both gate and drain were biased. As electrons transfer from source to drain and once the energy they gain can overcome the tunnel oxide barrier, they can charge and store in the floating gate, only around drain side. Shown in Fig. 5 are the transient programming characteristics of $NiSi_2$ nanocrystal memory. Figures 5 (a) and (b) show the drain bias and control gate bias effect on the programming efficiency, respectively. As increasing of either drain voltage or gate voltage, the programming gets faster and more charges are stored in the floating gate.

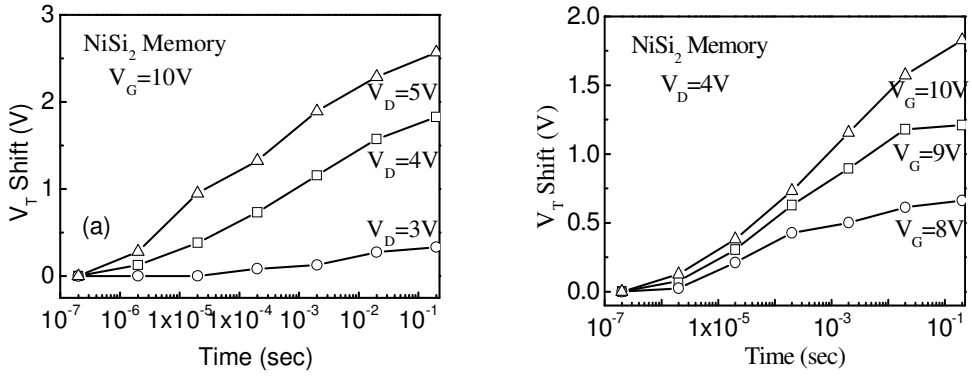

Figure 5 Hot carrier injection programming characteristics of $NiSi_2$ nanocrystal memory. (a) drain bias and (b) control gate bias dependence of the programming efficiency.

Since hot carrier can only locally inject to the floating gate, for example, to drain side if biasing drain and grounding source, the threshold voltage (V_T) shift is different between reading from drain side and source side. Figure 6 is the retention characteristics of HCI-programmed $NiSi_2$ nanocrystal memory under forward and reverse reading conditions. Three reading voltages were used for forward and reverse reading, therefore six retention curves are shown in the figure. Top three are reading from source side and bottom three are reading from drain side. Reading voltage affects the V_T only as reading from drain side because after HCI programming (biasing V_G and V_D), additional energy barrier was formed near the drain side for channel electrons. When reading from drain side, this barrier was lowered at larger read voltages, leading to different V_T shift.

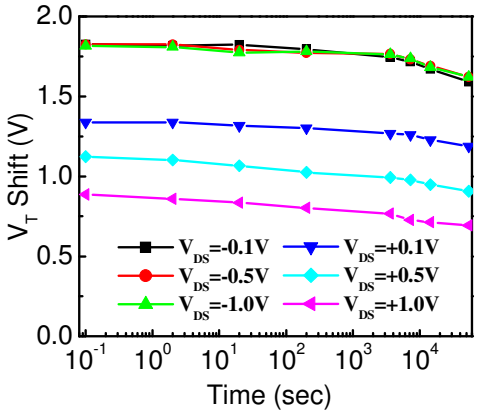

Figure 6 Retention characteristics of HCI-programmed $NiSi_2$ nanocrystal memory. Forward and reverse reads were used to sense the V_T shift.

CONCLUSIONS

Ni-catalyzed $NiSi_2$ nanocrystals were synthesized on thin oxide layer via VSS mechanism. Optimized conditions were obtained to get the silicide nanocrystals. MOSFET memory with $NiSi_2$ nanocrystals as the floating gate were characterized and good performance in terms of programming/erasing speed, long retention time and acceptable endurance were demonstrated.

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