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Performance enhancement of $TiSi_2$ coated Si nanocrystal memory device

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ABSTRACT

Self-aligned $TiSi_2$ coated Si nanocrystal nonvolatile memory was fabricated. This kind of MOSFET memory device is not only thermally stable, but also shows better performance in charge storage capacity, writing, erasing speed and retention characteristics. This indicates that CMOS compatible silicidation process to fabricate $TiSi_2$ coated Si nanocrystal memory is promising in memory device applications.

INTRODUCTION

The dimensions of Si based memory devices have approached the nanometer scale and Si nanocrystal embedded memory devices have significantly improved the performance of floating gate memory [1]. It was reported that the defects in Si nanocrystals boost up the long-term retention performance [2]. However, the defects based performance improvement is not stable in MOSFET memory device fabrication, in particular under subsequent high temperature annealing step [2]. New types of nanocrystal floating dots, such as double Si dots [3], Ge nanocrystals [4], metal [5-8] or metal-like [9] dots and dielectric nanocrystals (Al_2O_3, HfO_2, Si_4N_3, etc) [10-12], have been proposed to achieve memory devices with longer and stable retention performance. The higher defect levels in the dielectric require higher writing voltage, therefore inducing the erasing saturation [13]. A feasible solution to rule out the defect effect is to use nanocrystals with high density of states, such as metal nanocrystals [5-8], but the drawback of using Ge and metal nanocrystals is the inter-diffusion between nanocrystals and tunnel oxide during device integration [14-16]. The inter-diffusion degrades the tunnel oxide and worsens retention characteristics. Since the post annealing is necessary for most of the device process, the thermal stability of a memory cell has become very critical. In this work we proposed and experimentally verified a method to improve the thermal stability of the memory cell by using self aligned $TiSi_2$ coated Si nanocrystals technique. $TiSi_2$ coated Si nanocrystal memory can not only have faster writing/erasing speed, but also have longer retention performance than pure Si nanocrystal memory as a result of Fermi-level pinning effect and high density of states around the silicide.

EXPERIMENT

In device fabrication, first, 5 nm thermal oxide was grown in dry oxygen immediately followed by Si nanocrystal deposition. An ultra-thin (<0.5 nm) blanket Ti layer was then deposited. A modified two-step annealing for silicidation [17] was performed in nitrogen to coat the Si nanocrystals. The first annealing only forms silicide on Si nanocrystal and Ti on oxide remains as metal. After selectively removing the unreacted metal Ti, the wafer was annealed (second annealing) at 900 ^oC for 30 seconds to form thermally stable Si-rich silicide [18]. Control oxide of about 15 nm was then deposited, followed by a 350-nm-thick poly-silicon

deposition in Low Pressure Chemical Vapor Deposition (LPCVD). After the formation of gate pattern, the poly-silicon gate and source/drain regions were implanted with phosphorus followed by dopant activation.

RESULTS AND DISCUSSION

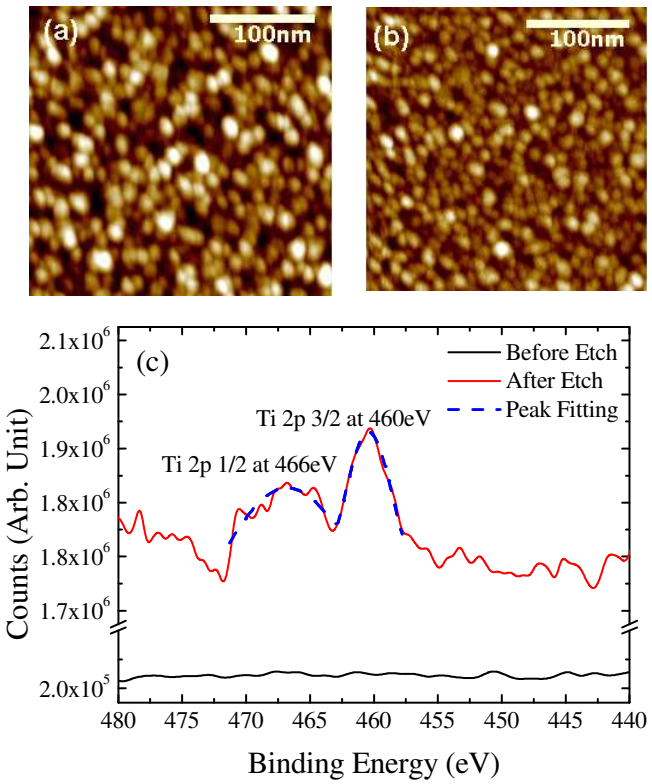

Fig. 1. AFM images of the $TiSi_2$ coated Si nanocrystals a) before and b) after diluted HF etching c) XPS result of the $TiSi_2$ coated Si nanocrystal sample before and after diluted HF etching

Figure 1(a) and (b) show the atomic force microscope (AFM) images of $TiSi_2$ coated Si nanocrystals before and after HF etching, respectively. The nanocrystal diameter is ~ 10 nm and the density is ~ 5×10^{11} cm^{-2}. The Si nanocrystals still exist after diluted HF etching, which indicates the fact that thin layer of Ti silicide has formed on the surface of the Si nanocrystals. Fig. 1(c) shows the results of X-ray photoelectron spectroscopy (XPS) of the same samples before and after HF etching. For the as-fabricated nanocrystal sample, there is one evident peak at 460 eV corresponding to Ti 2P3/2 states of $TiSi_2$. This Ti-related signal disappears after HF etching, which means the $TiSi_2$ portions of the nanocrystals were removed. The combination of AFM and XPS results suggests that $TiSi_2$ coated Si nanocrystals have been achieved.

To verify the details of coated shape of the nanocrystals, simple calculation was performed. A half circle shape of Si nanocrystal with height of 8nm and diameter of 16nm was proposed to deposit on SiO_2, as shown in Fig. 2 (a). Silicide process is suppressed by stress between SiO_2 and Si [19], here we assume the stress σ decreases as it is away from SiO_2: $\sigma_{nn} = Ae^{\frac{B}{n^2}}$.

Combining the concentration differential equation and stress related equation [20], the thickness of $TiSi_2$ is given by

$$\delta(THK) = \frac{\Delta t \times C \times k_s}{N_1}, \qquad k_s = k_{s0} \exp\left(-\frac{E_{k0} + \sigma_{nn} * V_{kp}}{k * T}\right)$$

Where Δt is the annealing time, C is the concentration of elements, K_S is the reaction rate, N_1 is the number of silicon atoms penetrating to the silicide layer, K_{S0}, E_{K0}, V_{KP} are parameters of the model. Fig 2 (b) shows the 2 dimension (2D) picture of $TiSi_2$ distribution in this structure. Si shows higher diffusion rate when it is away from the interface between Si and SiO_2. While at the edge of Si nanocrystal, slower diffusion rate results in the crescent shape of the coated $TiSi_2$.

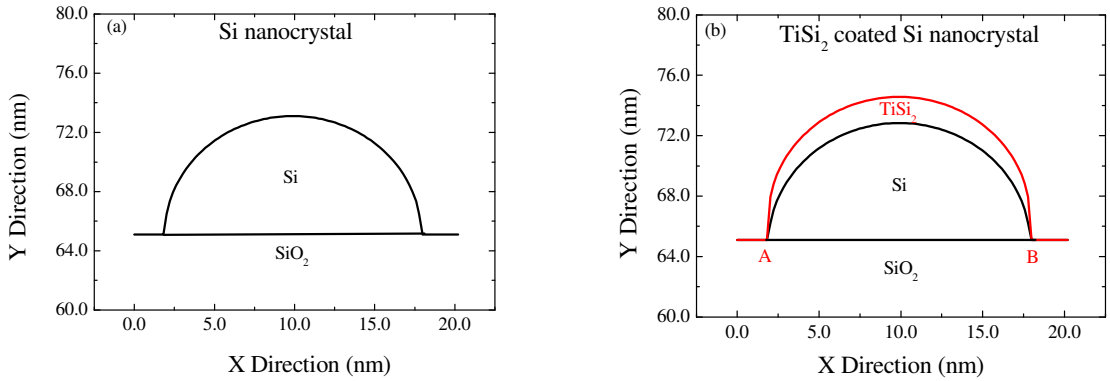

Fig. 2. a) Nanocrystal structure in the beginning of calculation, b) $TiSi_2$ signal distribution in 2D.

Figure 3(a) shows the schematic of $TiSi_2$ coated Si nanocrystal memory device. The blue color shows the Si nanocrystal and the orange ring covering the surface of Si nanocrystals represents $TiSi_2$ layer. Fig. 3(b) shows the 3D conduction band of $TiSi_2$ coated Si nanocrystal memory device. $TiSi_2$ layer which has lower energy level attaches the tunnel oxide and exists between control oxide and Si nanocrystals. Under writing, the electrons from Si substrate go through the tunnel oxide, Si nanocrystal and finally are confined in the $TiSi_2$ region.

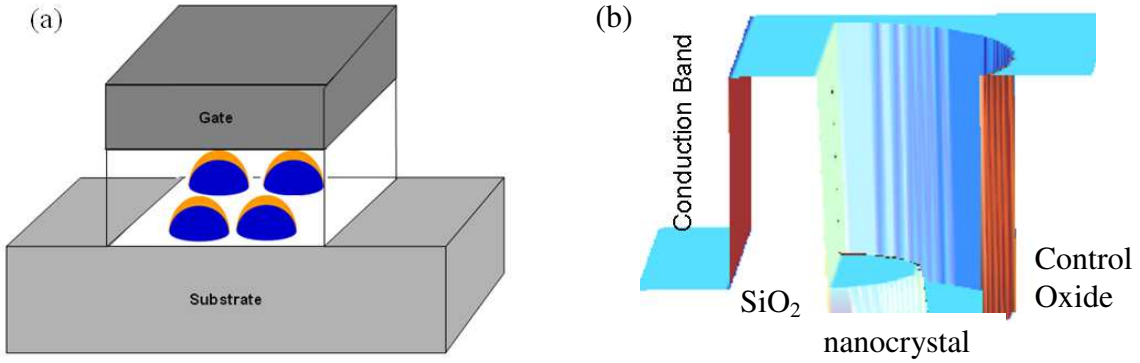

Fig. 3. (a) Schematic of $TiSi_2$ coated Si nanocrystal memory device, (b) Schematic of 3D conduction band structure of $TiSi_2$ coated Si nanocrystal memory device.

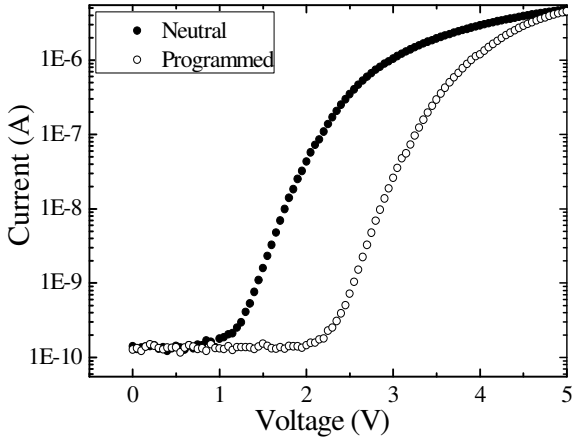

Fig. 4. Memory effect from $TiSi_2$ coated Si nanocrystal memory cell. The shift of I_{ds}-V_g curve after writing operation indicates the electron storage in the floating gate.

The devices were characterized by HP 4155A semiconductor analyzer and Agilent LCR meter at room temperature. Memory effect was clearly found for the memory device with $TiSi_2$ coated Si nanocrystals, as shown in Fig.4, where the source-drain current (I_{ds}) as a function of gate voltage (Vg) is shown for the neutral state and programmed state, respectively. The programming was performed at 20 V for 1 s. The shift (~1.2 V) of the I-V curve towards higher gate voltage indicates the electron storage in the nanocrystals.

The threshold voltage shift as a function of writing time and writing voltage is shown in Fig. 5 (a) and Fig. 5 (b), respectively. It is found that the memory window becomes saturated as the writing time elapses with Vg fixed at 15 V. This is due to the Coulomb blockade effect caused by the small nanocrystal size. The saturated memory window for the device with $TiSi_2$ coated Si nanocrystals is higher than the Si nanocrystal memory device. The saturation level increases with writing voltage which is shown in Fig. 5 (b). It is interesting to note in Fig.5 (b) that the threshold voltage shift exhibits an obvious difference between $TiSi_2$ coated Si

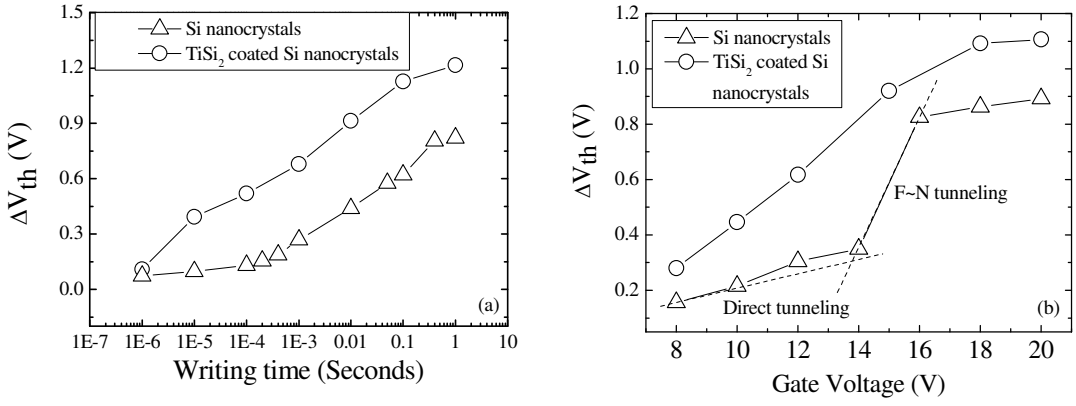

Fig. 5. Threshold voltage shift as a function of a) writing time and b) writing voltage, for memory cells with $TiSi_2$ coated Si nanocrystals and reference Si nanocrystals.

nanocrystal and Si nanocrystal memory devices. This is attributed to the different charge injection mechanisms in the two kinds of devices. In $TiSi_2$ coated Si nanocrystal case, $TiSi_2$ layer attaches the tunnel oxide and has lower energy level compared to the reference Si nanocrystals. The charge injection has already established through Fowler–Nordheim (F-N) tunneling at the voltage around 8V. $TiSi_2$ coated Si nanocrystals have more charges to be stored in the silicide because of its higher density of state (DOS). In Si nanocrystals, the energy levels are higher than that of $TiSi_2$ layer and the tunneling is direct tunneling at the voltage below 14V and F-N type at the voltage larger than 14V. As writing voltage increases further (>16 V), both devices become saturated.

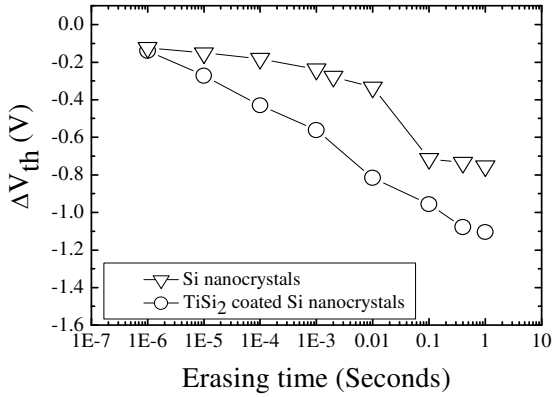

Fig. 6. Threshold voltage shift as a function of erasing time for memory cells with $TiSi_2$ coated Si nanocrystals and reference Si nanocrystals.

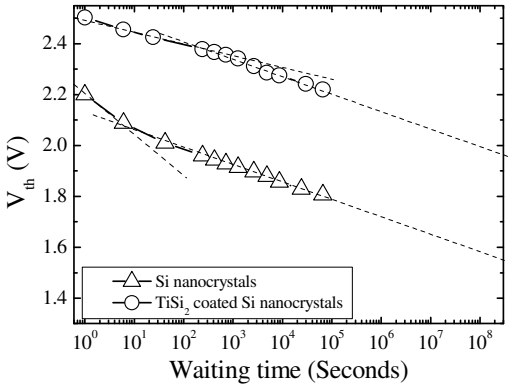

Fig. 7. Retention performance comparison between a reference Si nanocrystal and $TiSi_2$ coated Si nanocrystal memory devices. The writing was done at 20 V for 1s.

The threshold voltage shift as a function of erasing time at the erasing voltage of -15V is shown in Fig.6. The erasing is found speeding up with the increase of the erasing time in both samples. $TiSi_2$ coated Si nanocrystal memory shows higher erasing speed. In the $TiSi_2$ coated Si nanocrystal memory device, two factors make the erasing speed faster than the Si nanocrystal case: First, crescent shape of $TiSi_2$ layer makes the point discharge possible in the sharp area of the $TiSi_2$ layer. Second, tunnel oxide endures larger potential drop in the $TiSi_2$ coated Si nanocrystal, which helps electrons to go through by F-N tunneling.

The retention characteristics are shown in Fig. 7 for the two devices with $TiSi_2$ coated Si nanocrystals and reference Si nanocrystals, respectively. These devices were programmed at 20 V, with an initial memory window of ~1.27V and 0.9V respectively. $TiSi_2$ coated Si nanocrystal memory shows slower charge loss rate in earlier retention stage. In this case, the electrons stay in the $TiSi_2$ channel and most of them have the lower energy level which is difficult to go through the tunnel oxide layer. The other reason is that the interface between the $TiSi_2$ and tunnel oxide has very small area which is blocked by the coulomb blockade effect and results in the difficulty of leakage. After the extrapolation of the curves to 10 years at room temperature, the remaining memory window is predicted to be 0.65 V, which means 52% charge left, while that is only 0.25 V, which means only 28% charges left for the reference Si nanocrystal memory device, as can be seen from Fig. 7.

CONCLUSIONS

In summary, we have successfully fabricated $TiSi_2$ coated Si nanocrystal devices by self-aligned silicidation method. Due to $TiSi_2$ induced lower energy levels, the charge storage occurs mainly in the $TiSi_2$ layer. Therefore, as compared to the reference Si nanocrystal memory, the memory device with $TiSi_2$ coated Si nanocrystals shows a larger charge storage capacity, higher writing and erasing speed and much better retention performance.

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