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Thin Solid Films 518 (2010) S262–S265

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Self-assembled Ge/Si hetero-nanocrystals for nonvolatile memory application

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ARTICLE INFO

Available online 21 October 2009

Keywords:
Self-assembly
Ge/Si hetero-nanocrystal
MOS memory

ABSTRACT

In this work, Ge/Si hetero-nanocrystals are used as floating gates for nonvolatile memory application. The nanocrystals were fabricated by Ge selective growth on Si nanocrystals in a chemical vapor deposition system. The scanning electron microscopy measurement affirms the density and size of the nanocrystals to be $6\times10^{11}\,\mathrm{cm}^{-2}$ and 7 nm, respectively. Metal-oxide-semiconductor memory with Ge/Si hetero-nanocrystals and Si nanocrystals were fabricated and characterized. Significant hole retention enhancement was observed in Ge/Si hetero-nanocrystal memory. This performance enhancement is attributed to the quantum well formed between Ge and Si valance band, where holes are preferentially stored.

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1. Introduction

Nanocrystals have been investigated for the application of floating gate memory since they were first reported by S. Tiwari in 1996. Nanocrystal memory devices with electrically discrete nanodots as storage elements have exhibited great potential in dealing with the memory device scaling issue. Compared to conventional flash memory the nanocrystal memory operates at lower voltage with faster programming/erasing speed because the charge loss through lateral paths is suppressed by localizing the charge into electrically discrete nodes to enable thinner tunneling oxide for memory device. Silicon [1,2], germanium [3,4] and metal nanocrystals [5,6] embedded in dielectric layers have been widely studied for the nonvolatile memory application. Ten-year non-volatility is of primary importance for nonvolatile memory, however the trade-off between long retention time and faster operation speed prevents further scaling of the tunneling oxide. In this paper, Ge/Si hetero-nanocrystals (HNCs) were employed as the charging nodes to achieve a better retention performance than Si nanocrystal memory without degrading the program efficiency. Type II band alignment of Si and Ge makes it possible to localize the holes into Ge quantum well so that during retention, Si nanocrystal acts as an additional barrier to the tunneling oxide to prevent the holes stored in the Ge nanocrystals from tunneling back to the channel, thus a longer retention time is expected. In other words, to maintain the reasonable retention, a thinner tunneling oxide could be used, which enables faster programming/erasing speed. Simulation works have been done and shown the better performance of Ge/Si hetero-nanocrystal memory [7,8].

2. Experiment

n-Si (100) was used as the substrate because the Ge/Si hetero-nanocrystal memory is designed for p-channel device for superior performance of holes storage. After diffusion cleaning, a tunneling oxide of 5 nm was thermally grown at 850°C followed by 900°C in-situ annealing in N_2. This nitridation process can suppress the leakage path through some weak points in the SiO_2 layer. After tunneling oxide growth the wafer was transferred to a low pressure chemical vapor deposition (LPCVD) furnace. Si nanocrystals were first deposited at 600°C for 15 s, then Ge nanocrystals were selectively grown on top of Si nanocrystals at 400°C. Another thin Si cap layer was deposited at about 500°C to protect the Ge from being oxidized in the following control oxide deposition. Essentially our nanocrystals are more like Ge/Si core/shell nanostructure. Control oxide of about 25 nm was deposited at 400°C. Aluminum was evaporated and patterned as the contacts. The device characterization was carried out by Agilent 4284A Precision LCR meter to sense the flat band voltage and Agilent 81104A pulse/pattern generator to program/erase. Two reference devices (silicon nanocrystal memory running the same process as Ge/Si HNC memory except the Ge growth step and a MOSFET device without nanocrystal embedded) were fabricated in parallel.

3. Results and discussion

The device structures and energy band diagrams of Ge/Si HNC and Si NC memories are summarized in Table 1. In program, holes are injected from the channel to the Ge nanocrystal for Ge/Si HNC memory and Si nanocrystal for Si NC memory. In erase, either holes stored in the nanocrystals tunnel back to the channel or electrons in the channel tunnel into the nanocrystals to neutralize the holes. Considering the small effective mass and lower barrier to overcome, electrons tunneling into the nanocrystals dominates the erasing

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doi:10.1016/j.tsf.2009.10.103

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Table 1
Device structures and energy band diagrams of Ge/Si HNC and Si NC MOS memories under program, erase and retention modes.

	Device Structure	Energy Diagram (Program)	Energy Diagram (Erase)	Energy Diagram (Retention)
Ge/Si HNC Memory	CO (~25nm) TO (~5nm) Si/Ge/Si NC n-Si (100) Al contact CO: control oxide TO: tunnel oxide NC: nanocrystal	Ge NC E_V Si NC Control Oxide Tunnel Oxide	Si NC Ge NC E_C E_V Tunnel Oxide Control Oxide	Ge NC E_V Si NC Control Oxide Tunnel Oxide
Si NC Memory	CO (~25nm) TO (~5nm) Si NC n-Si (100) Al contact CO: control oxide TO: tunnel oxide NC: nanocrystal	Si NC E_V Control Oxide Tunnel Oxide	Si NC E_C E_V Control Oxide Tunnel Oxide	Si NC E_V Tunnel Oxide Control Oxide

process. In retention, when no bias is applied, holes are expected to stay longer in the Ge/Si HNC than Si NC since in Ge/Si HNC, there exists a double barrier, including tunneling oxide and the Si underneath the Ge, to prevent holes from leaking to the channel.

Fig. 1 shows the *C–V* sweep characteristic of Ge/Si HNC p-MOS memories. Inset is the scanning electron microscope (SEM) image of Ge/Si HNCs. The density and average size of the dots reading from this image are $6\times10^{11}\,\text{cm}^{-2}$ and 7 nm, respectively. Five devices (#1–#5) on a chip from center, top, down, left, and right side were tested. Table 2 summarizes the flat band voltage (V_{FB}) shift (memory window) of each device, and the average value of their memory window. The gate voltage scans from −15 V to 15 V and back to −15 V again. The V_{FB} shifts indicate clear holes charging effect.

Fig. 2 shows the *C–V* characteristic of Si NC p-MOS memories. Inset is the SEM image of Si NCs. The dot density and average size are $6\times10^{11}\,\text{cm}^{-2}$ and 6 nm, respectively. Table 3 summarizes the memory window for each device and their average value of the five devices tested. Similarly, V_{FB} shifts as gate voltage changes the scanning direction were observed. The average memory window of Ge/Si HNC memory is much larger than Si NC memory, indicating that Ge/Si HNC has larger storage capability. A control device without NCs in oxide was fabricated for comparison. As *C–V* sweeps, there is no hysteresis observed in this control device, which means the memory

Table 2
Memory window of Ge/Si HNC p-MOS memories, and their average value.

Ge/Si hetero-nanocrystal MOS memory						
Device number	#1	#2	#3	#4	#5	Average
Memory window (V)	3.029	2.991	2.263	2.723	2.915	2.784

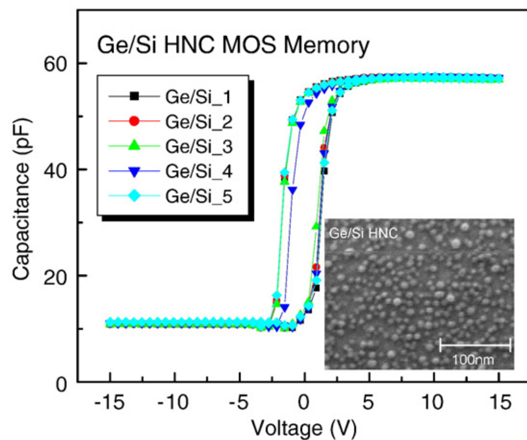

Fig. 1. *C–V* sweep of Ge/Si HNC p-MOS memories. Five devices from different areas of the chip were tested. Inset is the SEM image of Ge/Si HNCs.

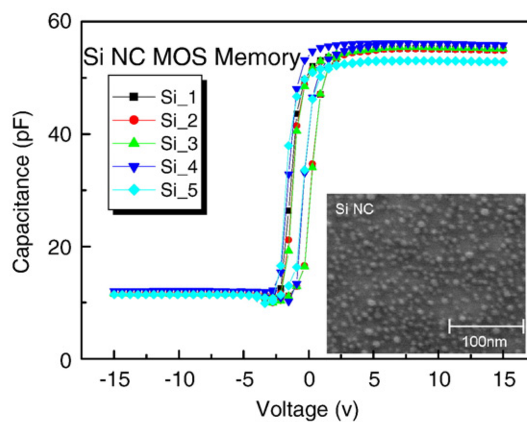

Fig. 2. *C–V* sweep of Si NC p-MOS memories. Five devices from different areas of the chip were tested. Inset is the SEM image of Si NCs.

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Table 3
Memory window of Si NC p-MOS memories, and their average value.

Si nanocrystal MOS memory						
Device number	#1	#2	#3	#4	#5	Average
Memory window (V)	1.563	1.433	1.495	1.237	1.433	1.425

effect in NC memory is actually due to the NC storage, rather than the defect/interface levels charging.

Similar dot density with bigger size of Ge/Si HNCs than Si NCs indicates the well-alignment of Ge and Si. This alignment was also confirmed by X-ray photoelectron spectroscopy (XPS) measurement [9]. Ge signals were clearly observed on the Ge/Si HNCs sample, while no such peaks were observed in Si NCs sample and the control device with no NCs in oxide matrix.

Fig. 3 shows the programming characteristic of Ge/Si HNC memory under different gate bias. Table 4 summarizes the V_{FB} shift after programming of the devices for 2 s. Fig. 4 shows the erasing characteristics under the various gate biases. Table 5 shows the V_{FB} shift after erasing. Agilent 81104A pulse/pattern generator was used to program/erase the device. Gate bias of −20 V/2 s was applied to charge the device with holes and 5 V/2 s to 12 V/2 s to discharge the device. In programming, holes tunnel from the channel to the Ge side of HNC and store there, leading to a left shift of V_{FB}, while in erasing with positive gate bias, holes become less as they are neutralized by electrons injected from the channel so that V_{FB} shifted to the right. The V_{FB} shift, i.e., memory window increases with the program bias confirms that the memory effect is from NC storage, rather than defect charging. A memory window of 0.427 V increases to 2.747 V as program bias increases from −14 V to −20 V, for 2 s. Similarly at the erase bias of 5 V/2 s, V_{FB} shifted 0.26 V back from the programmed status. As erase bias increases to 12 V/2 s, a 3.005 V shift was observed. The reason that erasing seems to consume less power is that electrons charging from accumulation region in the channel to the NCs dominate the erase process.

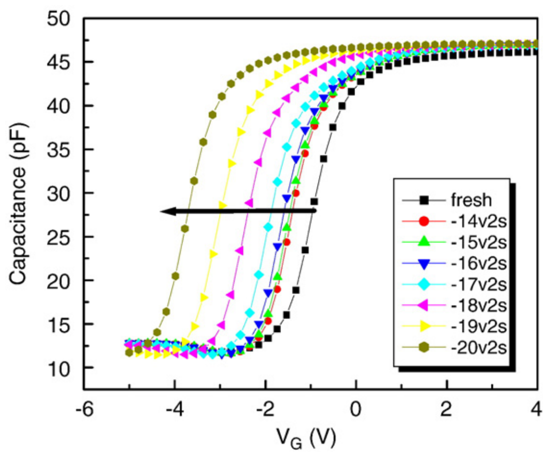

Fig. 3. Programming characteristics of Ge/Si HNC memory under different gate biases.

Table 4
V_{FB} shifts after programming.

Program *V* (V)	V_{FB} shift (V)
−14	0.427
−15	0.453
−16	0.613
−17	0.907
−18	1.413
−19	2.027
−20	2.747

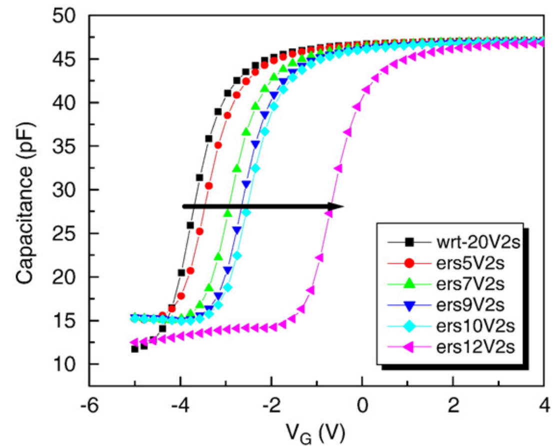

Fig. 4. Erasing characteristics of Ge/Si HNC memory under different gate biases.

Fig. 5 shows transient programming characteristics of Ge/Si HNC memory under −19 V program. Table 6 shows the V_{FB} shift at various program times. The clear V_{FB} shift, 0.312 V took place at 100 µs charging and saturated to 2.184 V at 2.1 s. Fig. 6 shows transient erasing characteristics of Ge/Si HNC memory under 12 V. Table 7

Table 5
V_{FB} shifts after erasing.

Erase *V* (V)	V_{FB} shift (V)
5	0.26
7	0.78
9	1.04
10	1.185
12	3.005

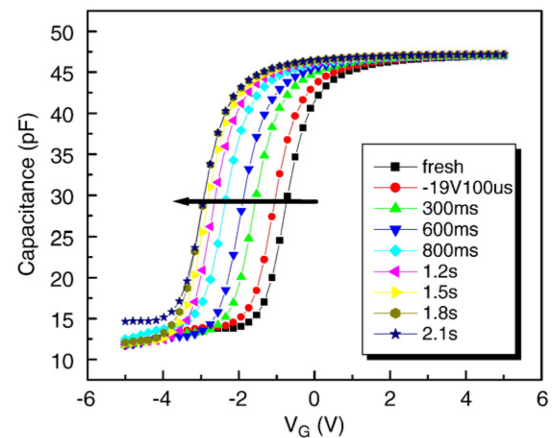

Fig. 5. Programming characteristics of Ge/Si HNC memory under different programming times.

Table 6
V_{FB} shifts after programming.

Program time (s)	V_{FB} shift (V)
1×10^{-4}	0.312
3×10^{-1}	0.832
6×10^{-1}	1.144
8×10^{-1}	1.629
1.2	1.907
1.5	2.08
1.8	2.184
2.1	2.184

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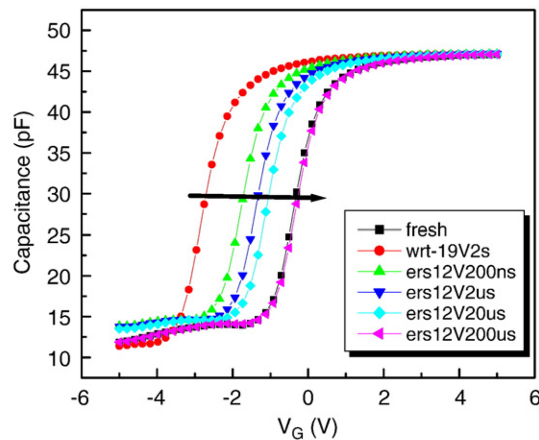

Fig. 6. Erasing characteristics of Ge/Si HNC memory under different erasing times.

Table 7
V_{FB} shifts after programming.

Erase time (s)	V_{FB} shift (V)
2×10^{-7}	0.971
2×10^{-6}	1.387
2×10^{-5}	1.63
2×10^{-4}	2.427

shows the V_{FB} shift at various erasing times. After 200 ns erasing, the V_{FB} shifted 0.971 V from the programmed state and back to the initial value at 20 µs.

Fig. 7 shows the retention characteristics of Ge/Si hetero-nanocrystal and Si nanocrystal MOS memory devices. After being charged at gate voltage of −20 V for 2 s the transient capacitance (C_t) was recorded every 0.03 s. V_{FB} shifts are converted by subtracting the voltage at C_t on the fresh C–V curve from the initial V_{FB} where the capacitance starts to be recorded. It is shown that after 10^4 s, the percentage of charge loss of Ge/Si HNC memory is half of that of the Si NC memory, which is due to the additional barrier formed by Si NC to prevent the holes in Ge NCs tunneling back to the channel. The charge decay for Ge/Si HNC and Si NC memory is a bit fast due to the stress (read voltage) applied on the gate as C_t being recorded.

4. Conclusion

Ge/Si self-assembled hetero-nanocrystals with a density of 6×10^{11} cm^{-2} were grown using LPCVD and MOS memory devices with Ge/Si hetero-nanocrystals and Si nanocrystals were fabricated

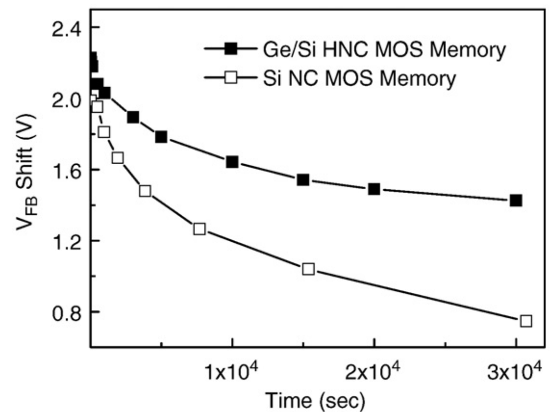

Fig. 7. Retention characteristics of Ge/Si HNC and Si NC MOS memories.

simultaneously. The memory window of Ge/Si hetero-nanocrystal device under ±15 V scanning is 2.784 V, which is twice of the Si nanocrystal memory. The charge decay of Ge/Si hetero-nanocrystal memory is much slower than Si nanocrystal memory. Using Ge/Si hetero-nanocrystals does not degrade the programming/erasing speed. Clear V_{FB} shifts were observed in Ge/Si hetero-nanocrystal memory after 100 µs programming and 200 ns erasing. This study suggests that Ge/Si hetero-nanocrystal memory may be a more promising candidate than Si nanocrystal memory in the future nonvolatile memory technology.

Acknowledgements

The authors acknowledge the financial and program support of Focus Center Research Program (FCRP) on FENA, the NSF (DMR-0807232, ECCS 0725630) and the Defense Microelectronics Activity (DMEA) under agreement number (H94003-09-2-0901).

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